IR-2541 DIV (2-3590)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS AND INTERFERENCES

In re Patent Application of	New York, New York
Daniel M. Kinzer et al.	Date: May 3, 2005
Serial No.: 10/613,326	Group Art Unit: 2811
Filed: July 3, 2003	Examiner: Q. D. Vu

For: VERTICAL CONDUCTION FLIP-CHIP DEVICE WITH BUMP CONTACTS ON SINGLE SURFACE

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF PURSUANT TO 37 C.F.R. §1.192

Sir:

This appeal is from the Examiner's final rejection of this application.

I. REAL PARTY IN INTEREST

The real party in interest in the above-identified application is:

International Rectifier Corporation

II. RELATED APPEALS AND INTERFERENCES

The applicant(s), the assignee(s) and the undersigned attorneys are not aware of any related appeals and interferences.

III. STATUS OF CLAIMS

Claims 1, 3-10, 12 and 14-20 are pending and on appeal herein.

Claims 27-29 are withdrawn without prejudice and not submitted for consideration on appeal.

Claims 2, 11, 13, and 21-26 have previously been canceled without prejudice.

IV. STATUS OF AMENDMENTS

An amendment was filed on February 3, 2005 to cancel claims 27-29.

The status of that amendment has not been reported to the applicants' attorneys.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is directed at a semiconductor device, and more particularly a power semiconductor device, which is configured for flip chip mounting. That is, a device according to the present invention as claimed has one surface which includes electrodes for power connection as well as an electrode for receiving control signals. More specifically, the device claimed is a power MOSFET which includes a source electrode, a drain electrode, and a gate electrode on the first major surface thereof.

A device according to claim 1, further includes another metallized layer on the surface opposite to the first major surface. This metallized layer is provided to help in dissipating the heat that is generated by the device during operation.

Thus, claim 1 calls for the following combination of features:

> 1. A flip chip semiconductor device comprising a silicon wafer having parallel first and second major surfaces; at least one P region and at least one N region in said wafer which meet at a PN junction within said silicon wafer; first and second coplanar, laterally spaced and metallized layers formed on said first major surface and insulated form one another and connected to said P region and said N region respectively; a bottom metallized layer extending across said second major surface; and
>
> a third metallized layer atop said first major surface which is coplanar with and laterally spaced from said first and second metallized layers; said first, second and third metallized layers comprising source, drain and gate electrodes respectively of a MOSgated device.

A device according to claim 12 further calls for a plurality of contact bumps for the first power electrode, and a plurality of contact bumps for the second power electrode. The bumps on the first electrode are disposed along a first straight row and the bumps on the second power electrode are disposed along a second straight row. By aligning the bumps along straight lines as set forth in claim 12, "the respective conductive traces on the printed circuit board receiving the device can be laid out in simple straight lines." See specification at page 8, lines 13-15.

Claim 12, therefore, calls for the following combination of features:

> 12. A flip chip semiconductor device comprising a silicon wafer having first and second parallel major surfaces; at least one P region and at least one N region in said wafer which meet at a PN junction within said silicon wafer; first and second coplanar, laterally spaced metallized layers formed on said first major surface and insulated form one another and connected to said P region and said N region respectively; a third metallized layer atop said first major surface which is coplanar with and laterally spaced from said first and second metallized layers; said first, second and third metallizing layers comprising source, drain and gate electrodes respectively of a MOSgated device; and a plurality of contact bumps connected to each of said first and second metallized layers; said plurality of contact bumps connected to said first metallizing layer being aligned along a first straight row; said plurality of contact bumps connected to said second metallizing layer being aligned along a second straight row.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claim 1 is anticipated by Vasquez et al. (Vasquez), U.S. Patent No. 5,578,841.

Whether claim 12 is obvious over Vasquez alone.

VII. ARGUMENT

Claims 1 and 12 both require a first, a second and a third metallized layer on the same surface. These metallized layers being the source, the drain and the gate of a MOSgated device.

Vasquez shows a "vertical MOSFET device 11". Col. 1, line 54. MOSFET device 11 includes gate electrode 23, col. 2, line 28, and two source electrodes 21, col. 2, line 44. Gate electrode 23 and source electrodes 21 are formed on the same surface 31.

Device 11 further includes drain electrode 26. Col. 4, line 65. Drain electrode 26 resides on surface 32. See Figure. Surface 31 and 32 are opposite one another. Col. 1, line 64.

In the Office Action dated November 3, 2004, regarding claim 1, the Examiner states the following:

> Vasquez et al. (figure 1) teach a flip-chip semiconductor device comprising a silicon wafer (34) having parallel first (an upper surface of the wafer [34]) and second (a bottom surface of the wafer [34]) major surfaces; at least one P region (P region in the epitaxial [17]) and at least one N region (N region in the channel [14]) in the wafer which meet at a PN junction within the silicon wafer (34); first (21 is located on the left side of figure 1) and second (21 is located on the right side of figure 1) are coplanar, laterally spaced and metallized layers (left [21]), right [21]) formed on the first (an upper surface of the wafer [34]) major surface and insulated from one another and connected to the P region and the N region respectively; a bottom metallized layer (26) extending across the second major surface (a bottom surface of the wafer [34]); and a third metallized layer (23) atop the first (an upper surface of the wafer [34]) major surface which is coplanar with and laterally spaced from the first (left [21]) and second right [21]) metallized layers; the first, second and third metallized layers comprising source, drain and gate electrodes respectively of a MOS gated device.

Thus, the Examiner has stated that one of the source electrodes 21 is actually a drain electrode. There is no support in Vasquez for the Examiner's position. Vasquez, therefore, does not anticipate claim 1. Claim 1 should, therefore, be allowed over Vasquez.

In the Office Action dated November 3, 2004, regarding claim 12, the Examiner states the following:

> Vasquez et al. (figure 1) teach a flip-chip semiconductor wafer (34) having parallel first (an upper surface of the wafer ([34])) and second (a bottom surface of the wafer [34]) major surfaces; at least one P region (P region in the epitaxial [17]) and at least one N region (N region in the channel [14]) in the wafer which meet at a PN junction within the silicon wafer (34); first (21 is located on the left side of figure 1) and second (21 is located on the right side of figure 1) are coplanar, laterally spaced and metallized layers (left [21], right [21]) formed on the first (an upper surface of the wafer [34]) major surface and insulated from one another and connected to the P region and the N region respectively; a third metallized layer (23) atop the first (an upper surface of the wafer [34]) major surface which is coplanar with and laterally spaced form the first (left [21]) and second (right [21]) metallized layers; the first, second and third metallized layers comprising source, drain and gate electrodes respectively of a MOS gated device; and a plurality of contact bumps (24) connected to each of the first (left [21]) and second (right [21]) metallized layers.

Again, the Examiner has stated that one of the source electrodes 21 is actually a drain electrode. There is no support in Vasquez for the Examiner's position. Furthermore, claim 12 calls for:

a plurality of contact bumps connected to each of said first and second metallized layers; said plurality of contact bumps connected to said first metallizing layer being aligned along a first straight row; said plurality of contact bumps connected to said second metallizing layer being aligned along a second straight row.

The Examiner has not provided a reference that teaches the latter limitations. Thus, the record does not support a basis for a *prima facie* case of obviousness, as it critically lacks a reference to teach the difference between the teachings of Vasquez as alleged by the Examiner and claim 12. Instead of a reference, the Examiner has only offered the following:

> It would have been obvious to one having ordinary skill in the art at the time the invention was made for the plurality of contact bumps connected to the first metallized layer being aligned along a first straight row and the plurality of contact bumps connected to the second metallized layer being aligned along a second straight row because it provides interconnection between the chip and the external device.

Claim 12 requires the bumps to be aligned along a straight line. The purpose of this feature is to enable the use of simple, straight tracks on a circuit board. The Examiner has not cited a motivation or suggestion in the prior art for such a feature.

It is respectfully submitted that for the above reasons, the record does not support a *prima facie* case of obviousness to reject claim 12.

The remaining claims are dependent claims and should be deemed allowable as depending from an allowable base claim.

VIII. CONCLUSION

Claims submitted herein for consideration on appeal are neither anticipated by nor obvious over Vasquez.

If this communication is filed after a shortened statutory time period has elapsed and no separate Petition is enclosed, the Commissioner of Patents and Trademarks is petitioned, under

37 C.F.R. §1.136(a), to extend the time for filing a response to the outstanding Office Action by the number of months which will avoid abandonment under 37 C.F.R. §1.135. The fee under 37 C.F.R. §1.17 should be charged to our Deposit Account No. 15-0700.

In the event the actual fee is greater than the payment submitted or is inadvertently not enclosed or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge the underpayment to Deposit Account No. 15-0700.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 3, 2005

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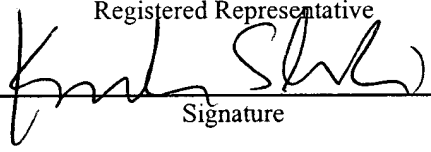

Signature

May 3, 2005
Date of Signature

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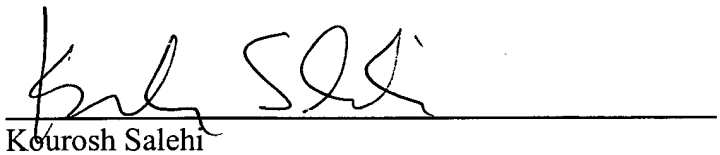
Respectfully submitted,



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CLAIMS APPENDIX

1. A flip chip semiconductor device comprising a silicon wafer having parallel first and second major surfaces; at least one P region and at least one N region in said wafer which meet at a PN junction within said silicon wafer; first and second coplanar, laterally spaced and metallized layers formed on said first major surface and insulated form one another and connected to said P region and said N region respectively; a bottom metallized layer extending across said second major surface; and

a third metallized layer atop said first major surface which is coplanar with and laterally spaced from said first and second metallized layers; said first, second and third metallized layers comprising source, drain and gate electrodes respectively of a MOSgated device.

Claim 2. (Canceled)

3 The device of claim 1 which further includes at least one contact bump connected to each of said metallized layers.

4 The device of claim 1 which further includes at least one contact bump connected to each of said metallized layers.

5. The device of claim 1 wherein said bottom metallized layer is substantially thicker than all of said first and second metallized layers.

6. The device of claim 1 wherein said bottom metallized layer is substantially thicker than all of said first and second metallized layers.

7. The device of claim 1 wherein said bottom metallized layer is substantially thicker than all of said first and second metallized layers.

8. The device of claim 4 wherein said bottom metallized layer is substantially thicker than all of said first and second metallized layers.

9. The device of claim 1 wherein a plurality of contact bumps are connected to each of said first and second metallized layers; said plurality of contact bumps connected to said first metallized layer being aligned along a first straight row; said plurality of contact bumps connected to said second metallized layer being aligned along a second straight row.

10. The device of claim 9 wherein said first and second rows are parallel to one another.

Claim 11. (Canceled)

12. A flip chip semiconductor device comprising a silicon wafer having first and second parallel major surfaces; at least one P region and at least one N region in said wafer which meet at a PN junction within said silicon wafer; first and second coplanar, laterally spaced metallized layers formed on said first major surface and insulated form one another and connected to said P region and said N region respectively; a third metallized layer atop said first major surface which is coplanar with and laterally spaced from said first and second metallized layers; said first, second and third metallizing layers comprising source, drain and gate electrodes respectively of a MOSgated device; and a plurality of contact bumps connected to each of said first and second metallized layers; said plurality of contact bumps connected to said first metallizing layer being aligned along a first straight row; said plurality of contact bumps connected to said second metallizing layer being aligned along a second straight row.

Claim 13. (Canceled)

14. The device of claim 12 further comprising a bottom metallized layer extending across said second major surface.

15. The device of claim 12 wherein said bottom metallized layer is substantially thicker than all of said first and second metallized layers.

16. The device of claim 12 wherein said first and second rows are parallel to one another.

17. The device of claim 12 wherein said silicon wafer is a rectangular wafer having an area defined by a given length and a given width, said length being greater than said width; said first and second rows of bumps being parallel to one another and being symmetric about a diagonal line across said wafer.

18. The device of claim 17 which includes a third metallized layer atop said first major surface which is coplanar with and laterally spaced from said first and second metallized layers; said first, second and third metallized layers comprising source, drain and gate electrodes respectively of a MOSgated device.

19. The device of claim 14 wherein said silicon wafer is a rectangular wafer having an area defined by a given length and a given width, said length being greater than said width; said first and second rows of bumps being parallel to one another and being symmetric about a diagonal line across said wafer.

20. The device of claim 12 which further includes a bottom metallized layer extending across said second major surface.

Claims 21.-26. (Canceled)

27. A semiconductor device comprising a silicon die having first and second parallel surfaces; a region of one conductivity type extending from said first surface and into the body of said die; a junction pattern defined in said device formed by a plurality of laterally spaced diffusions of the other conductivity type into said region of one conductivity type; a first conductive power electrode formed atop said first surface and in contact with said plurality of laterally spaced diffusions; a second conductive power electrode formed atop said first surface which is coplanar with and laterally spaced from and insulated from said first conductive electrode and in electrical contact with the body of said die through a high conductivity element located outside said region of one conductivity type; and at least one solder ball connector formed atop each of said first and second conductive electrodes respectively; the

current path from said first conductive electrode to said second conductive electrode having a vertical component which is generally perpendicular to said first surface.

28. A semiconductor device according to claim 27, wherein said high conductivity element is a sinker diffusion of higher conductivity than said body region.

29. A semiconductor device according to claim 27, wherein said high conductivity element is a metallic material residing in a trench formed in said body of said die.